Tutorial 2
Counters

Exercise 1

1. For the circuit shown in Figure 1, complete the timing diagram below.

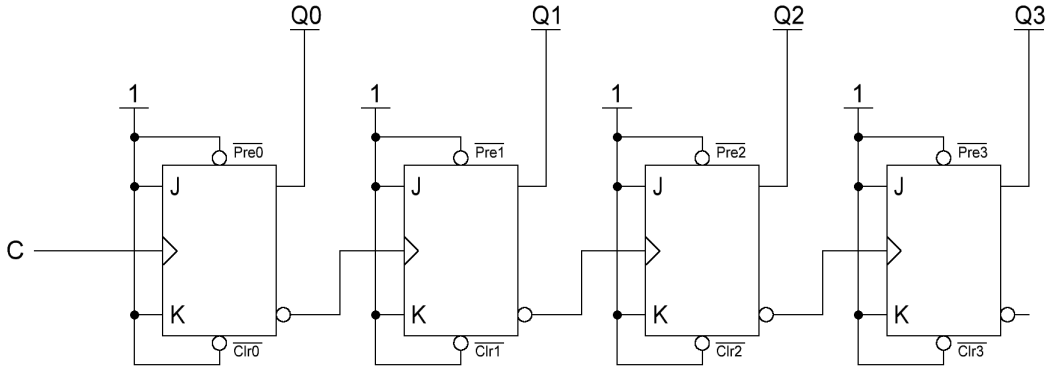
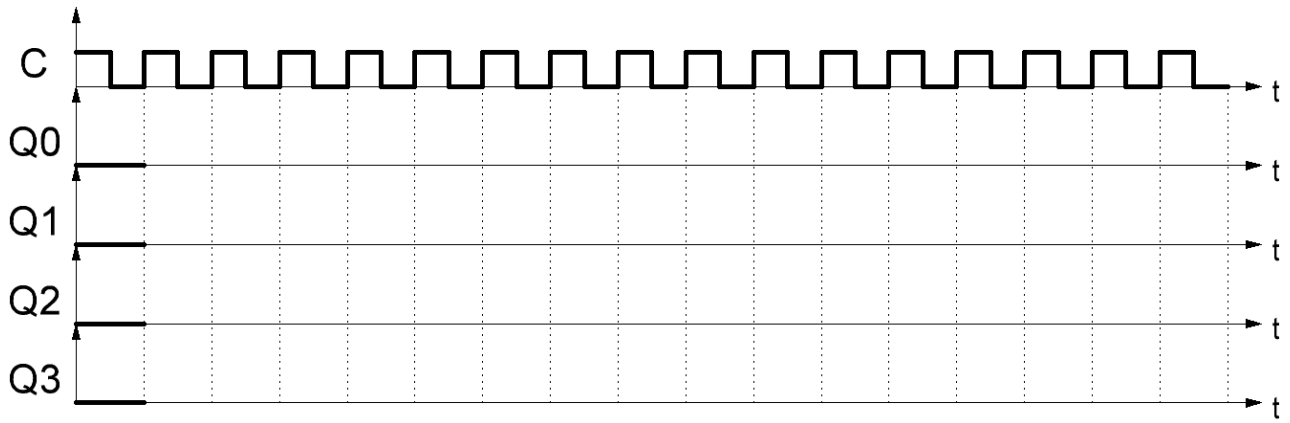


Figure 1



2. What does the circuit shown in Figure 1 do?

3. Slight changes are made to the circuit shown in Figure 1 in order to obtain the circuit shown in Figure 2. What does this new circuit do? Explain your line of reasoning.

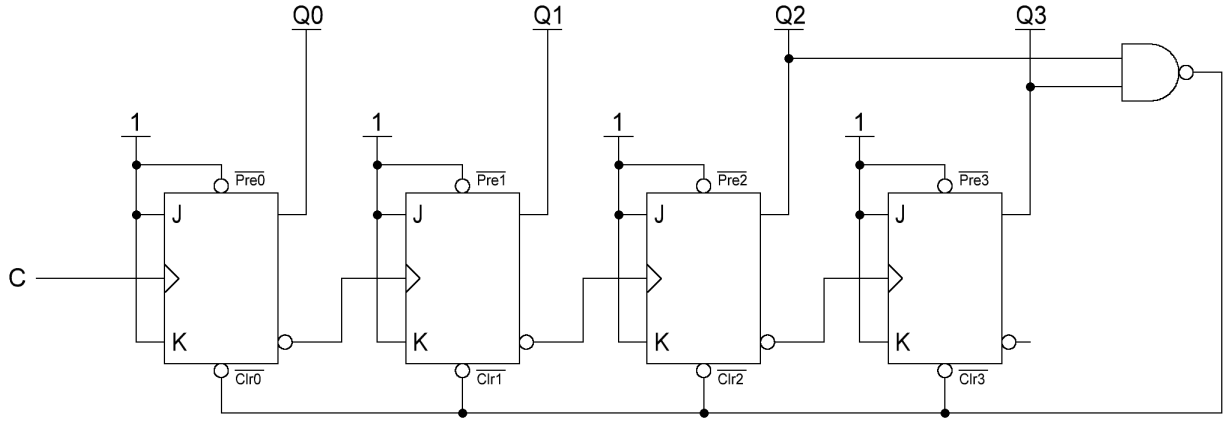


Figure 2

4. For the circuit shown in Figure 3, complete the timing diagram below.

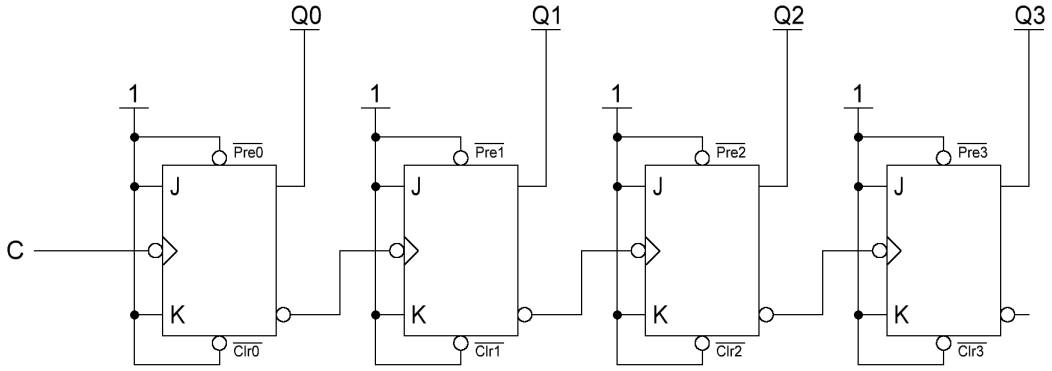
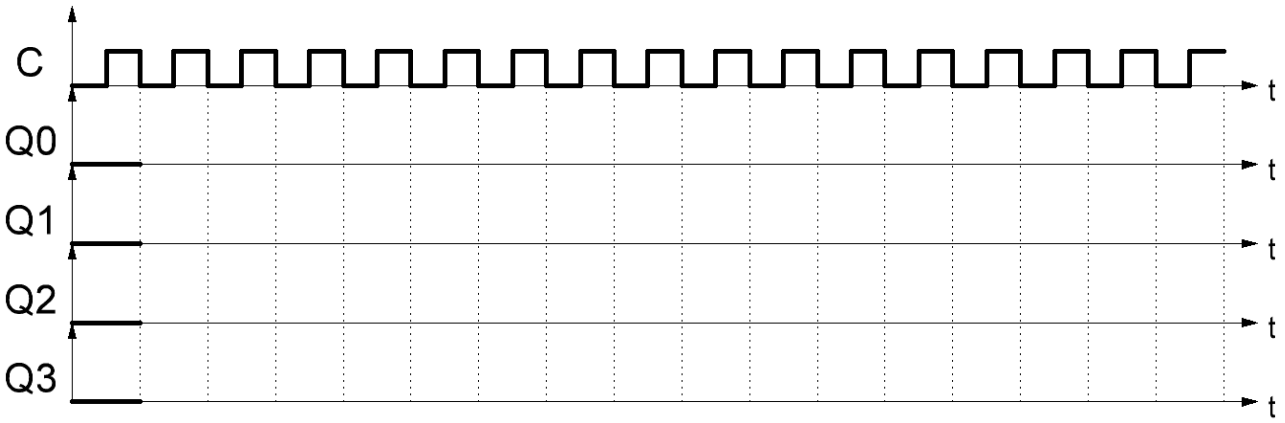


Figure 3



5. What does the circuit shown in Figure 3 do?

6. Slight changes are made to the circuit shown in Figure 3 in order to obtain the circuit shown in Figure 4. What does this new circuit do? Explain your line of reasoning.

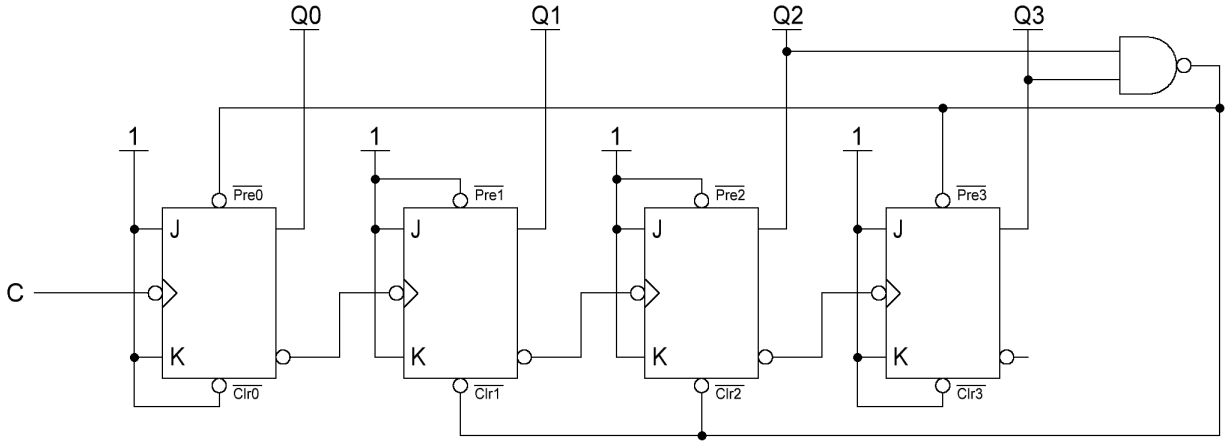
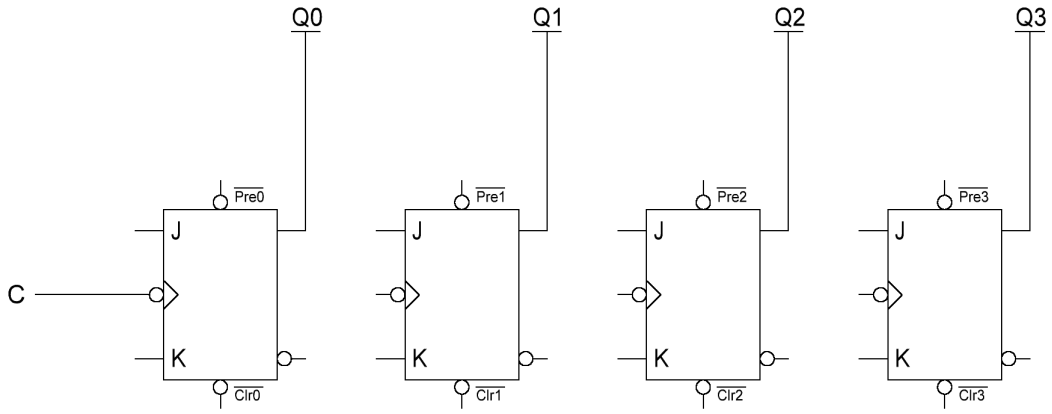
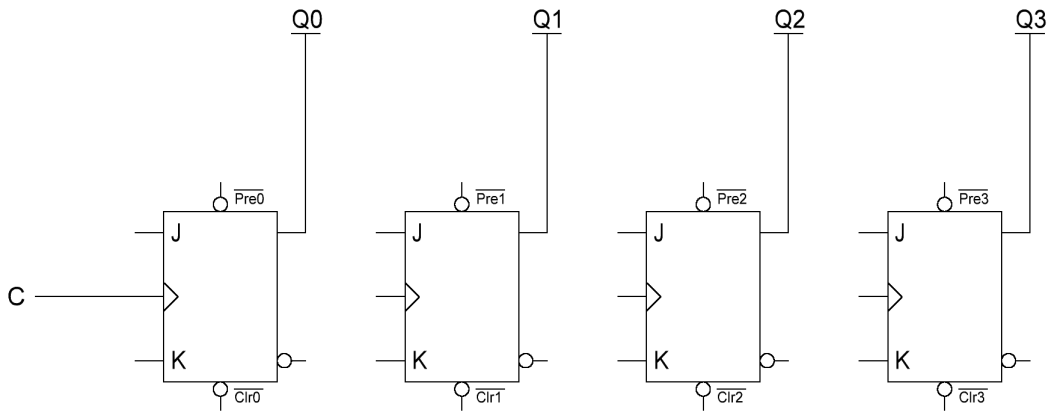


Figure 4

7. Wire the following flip-flops in order to design a modulo-10 asynchronous up counter.



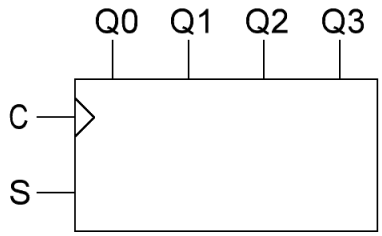
8. Wire the following flip-flops in order to design a modulo-13 asynchronous down counter.



Exercise 2

We want to design a modulo-16 up/down counter. That is to say, a circuit that has two different modes: an up-count mode and a down-count mode. The mode can be set with an *S* input:

- S = 0 → up-count mode.
- S = 1 → down-count mode.



Draw the circuit diagram of the modulo-16 up/down counter. Use only positive-edge-triggered JK flip-flops and logic gates.

Exercise 3

To begin with, you must design a modulo-7 synchronous counter using positive-edge-triggered JK flip-flops.

1. Using the excitation table of a JK flip-flop, complete the table below.

Q2	Q1	Q0	J2	K2	J1	K1	J0	K0

2. Obtain the most simplified expressions for *J0*, *K0*, *J1*, *K1*, *J2* and *K2*.
3. Draw the circuit diagram of the counter.

Then, you have to design a 3-bit synchronous Gray counter using negative-edge-triggered D flip-flops.

4. Complete the table below.

Q2	Q1	Q0	D2	D1	D0
0	0	0			
0	0	1			
0	1	1			
0	1	0			
1	1	0			
1	1	1			
1	0	1			
1	0	0			

5. Obtain the most simplified expressions for *D0*, *D1* and *D2*.
6. Draw the circuit diagram of the counter.

Lastly, you have to design the same 3-bit synchronous Gray counter but by using negative-edge-triggered JK flip-flops.

7. Complete the table below.

Q2	Q1	Q0	J2	K2	J1	K1	J0	K0

8. Obtain the most simplified expressions for *J0*, *K0*, *J1*, *K1*, *J2* and *K2*.

Exercise 4

Complete the timing diagram for the circuit below (*E = 0*).

